Silicon Power
INDUSTRIAL

Industrial
M.2 2280 SATA3 SSD
MDC350 S/R B+M key Series

Datasheet

Specifications Overview

- **Capacity**
  - 64GB, 128GB, 256GB, 512GB, 1TB, 2TB, 3.8TB
- **Form Factor**
  - M.2 2280 (B+M key)
- **Interface**
  - SATA III
- **Performance**
  - Sequential Read: up to 560 MB/s
  - Sequential Write: up to 515 MB/s
  - Random 4k Read: up to 92K IOPS
  - Random 4k Write: up to 81K IOPS
- **Temperature Range**
  - Operation temperature:
    Normal temperature: -20°C to +75°C
    Wide temperature: -40°C to +85°C
- **Power Consumption**
  - Supply Voltage: DC +3.3V ± 5%
  - Read (Max.): 720 mA
  - Write (Max.): 980 mA
  - Idle (Avg.): 200 mA
- **Reliability**
  - TBW:
    64GB: 176TB
    128GB: 352TB
    256GB: 704TB
    512GB: 1,408TB
    1TB: 2,816TB
    2TB: 5,632TB
    3.8TB: 11,264TB
  - MTBF: > 3,000,000 hrs
- **ECC Performance**
  - LDPC
- **Environment Specification**
  - Shock
  - Vibration
- **Compliant Specifications**
  - RoHS 2.0
- **Feature Support**
  - TCG OPAL 2.0
  - AES-256
  - Write Protect(Only BiCS4)
  - Secure Erase(Only BiCS4)

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Revision	Date	Major Changes
1.0	2019/01/22	1. Formal release.
1.1	2019/03/19	1. Update 512GB Data.
1.2	2019/11/25	1. Modify document layout
1.3	2019/12/13	1. Add 064GIMDC355SV0-040
1.4	2019/12/18	1. Add 256GIMDC355RV0-010
1.5	2020/02/26	1. Add 010TIMDC351SW0-010
1.6	2020/05/18	1. Revise 64GB performance 2. Remove 064GIMDC355SV0-010 / 020 / 030 3. Add 064GIMDC355SV0-050
1.7	2020/08/10	1. Add SKUs ● 64GIMDC351SW0-010 ● 128GIMDC351SW0-010 ● 256GIMDC351SW0-010 ● 512GIMDC351SW0-010
1.8	2020/09/15	1. Remove Controller Name 2. Add RW0 SKUs (351RW) 3. Modify TBW Notice description 4. Revise Performance value 5. Add 010TIMDC355SV0-010
1.81	2020/09/25	1. Add 512GIMDC355SV0-040
1.9	2020/10/06	1. Modify TBW value 2. Revise Performance value
2.0	2021/03/17	1. Revise Power Consumption value 2. Revise Performance
2.1	2023/08/28	1. Update order information.
2.2	2023/12/21	1. Update temperature criterion.
2.3	2024/03/28	1. Update order information (BiCS5).
2.4	2024/08/28	1. Add 038TIMDC355SV0-010 2. Add MDC350R(BiCS5) series
2.5	2024/10/07	1. Add 128GIMDC355SV0-080 2. Add 256GIMDC355SV0-070 3. Add 512GIMDC355SV0-060 4. Add 010TIMDC355SV0-040 5. Add 020TIMDC355SV0-020
2.6	2024/10/24	1. Update temperature information

1. Product Description

1.1 Overview

Silicon Power's MDC350 series M.2 2280 SATA3 solid state disk is a storage device based on 3D NAND flash memory technology. The MDC350 series includes the following models to fulfill a variety of different demands:

- MDC350R Rugged series – external DRAM and dual secure design for power failure protection, including power-shielding firmware architecture protection and an advanced PFP circuit with industrial-grade polymer capacitors to combat sudden power-loss situations.
- MDC350S Performance series – external DRAM and power-shielding firmware architecture protection to manage sudden power-loss situations.

The MDC350 series is equipped with an LDPC ECC engine to guarantee 3K PE cycles endurance with 3D NAND. It also features the latest Direct-To-TLC and SLC cache firmware architecture and external DRAM to achieve the optimal sustained read/write performance and reduce Write Amplification to offer even better TBW endurance than 2D MLC models can offer.

StaticDataRefresh technology monitors the voltages and gives a quick refresh as needed to keep read performance high over time and maintain data integrity. Early weak block retirement and global wear leveling algorithm assures an equal usage of the flash memory cells to extend SSD lifespan.

The MDC350S/R series contains hardware write protection and a secure erase function via an optional connector feature. It can also provide software write protection and a secure erase function via software vendor commands, by request.

The MDC350S/R series is equipped with an integrated Industrial-grade Active PMU (power management unit) to provide higher reliability power design compared to traditional discrete circuits. It also features complete protection with OVP, OCP, Surge Rejection, and In-Out Short Protection to provide a higher level of protection versus traditional fuse design.

1.2 Features

- M.2 2280 standard form factor with Serial ATA standard interface connector
- Compliant with Serial ATA revision 3.1 standard with 6.0 Gb/s transfer rate
- Compliant with ATA/ATAPI-8 standard and ACS-3 command protocol
- Built-in-Voltage detector for power shielding protection and an advanced PFP function
- Native Command Queuing up to 32 commands
- Garbage collection and TRIM Data Set Management command
- Global wear leveling algorithm evens program/erase count
- Early weak block retirement
- Supports SMART feature command set
- Supports 28/48 bit LBA mode command
- Supports SATA DEVSLP for advanced power saving
- Built-in temperature sensor (Thermal Throttling) function to adjust access speed of NAND flash and keep the SSD system stable
- Supports real time Full Disk Encryption (FDE) with Advanced Encryption Standard (AES) 128/256-bit. strength(optional service)
- Supports Trusted Computing Group (TCG) Opal protocol(optional service)
- Supports in-field seamless FW update tool via USB interface to keep the SSD's original data (optional service)
- Optional Conformal Coating - Standard IPC A-610E
- Hardware Write Protect (optional service)
- Hardware Secure Erase triggering (optional service)

1.3 System Requirements

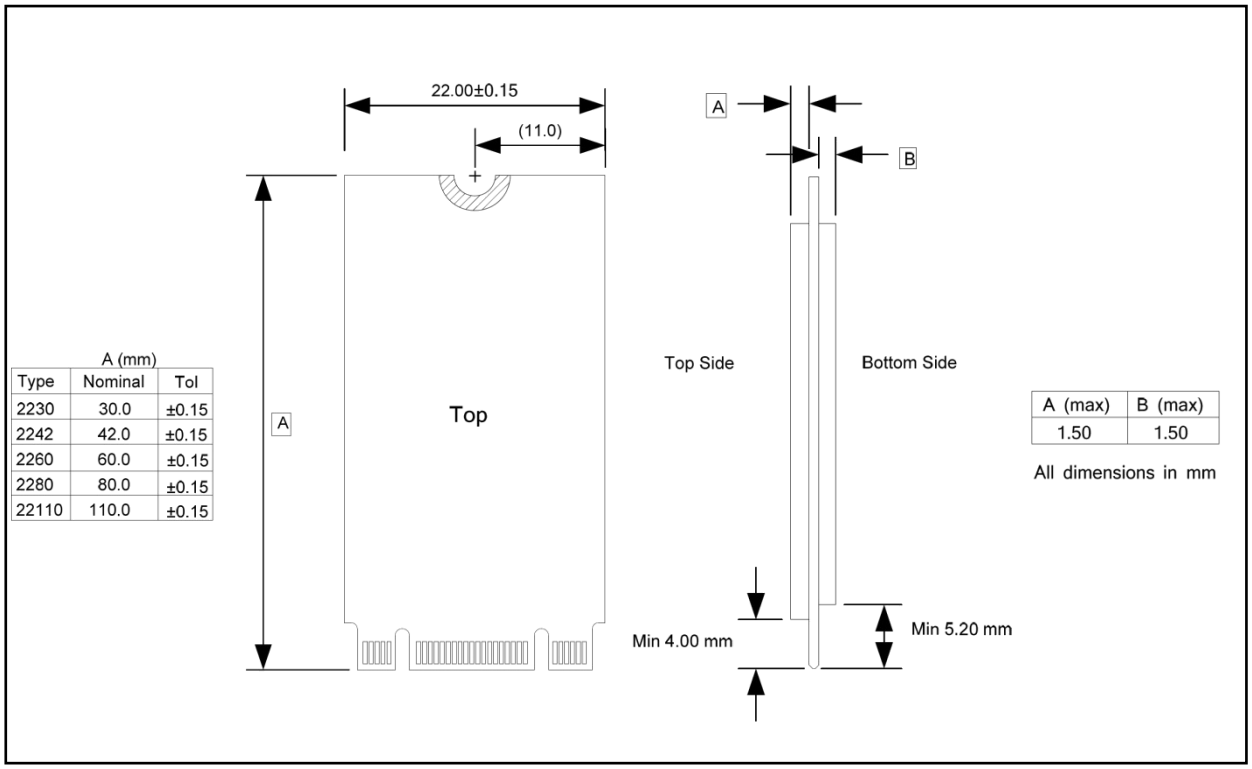
- SATA 6.0 Gb/s Interface, backward compatible with 1.5/3.0 Gb/s, SATA M.2 2280 standard form factor.
- Voltage: DC +3.3V ± 5%
- Operating System:
  - Windows
  - Linux

2. Specification

2.1 Physical Dimension

2.1.1 Dimension

The Dimensions of M.2 2280 SATA SSD are illustrated in Figure 1 and described in Table1.



A (mm)

Type	Nominal	Tol
2230	30.0	±0.15
2242	42.0	±0.15
2260	60.0	±0.15
2280	80.0	±0.15
22110	110.0	±0.15

A (max)	B (max)
1.50	1.50

Figure 1 : M.2 2280 SATA SSD Dimensions with 7mm thickness

Table 1 : M.2 2280 SATA SSD Physical Dimension

Length	80±0.15mm
Width	22±0.15mm
Thickness(connector)	3.5mm

2.1.2 Weight

Mode	Weight						Unit
	128GB	256GB	512GB	1TB	2TB	3.8TB	(± 5%)
R series	7.5	7.7	8.0	8.5	8.5	9.0	g
S series	6.0	6.2	6.5	7.0	7.0	7.5	g

2.2 Electrical Specifications

2.2.1 Operating Condition

- Supply Voltage: DC +3.3V ± 5%

Table 2 : Power Consumption

Mode	Power Consumption							Unit
	64GB	128GB	256GB	512GB	1TB	2TB	3.8TB	
Read (Max)	450	505	685	680	690	700	720	mA
Write(Max)	420	540	730	780	780	800	980	mA
Idle (Avg.) (S series)	120	160	300	300	300	300	300	mA
Idle (Avg.) (R series)	340	340	340	340	340	340	340	mA

Notice: The value is various bases on the capacity and the test platform.
Notice: Power consumption is measured during the sequential read and write operations performed by CrystalDiskMark.
Notice: Power consumption of Idle is measured when the platform gets into a steady-state mode after IOMeter runs "Idle" script for 10mins.

※Testing Platform: Test PC: MSI-Z87-G45 GAMING, CPU: Intel(R) Dual-Core i5-4430 CPU 3.0GHz, Memory: DDR3-1600 2GB X 2pcs, Testing OS: Windows 7 32 Bit, Testing Software: Crystal Disk Mark 5.5.0, Test Temperature: 25°C

2.2.2 External DRAM information (MDC350S&R series)

- Type: DDR3

2.2.3 LED signal definitions

- D6 : Power – to indicate the power-on status.
- D3 : Controller Activity – to indicate the controller working status
- D2 : Data activity to SATA interface – to indicate the data access activity on SATA interface

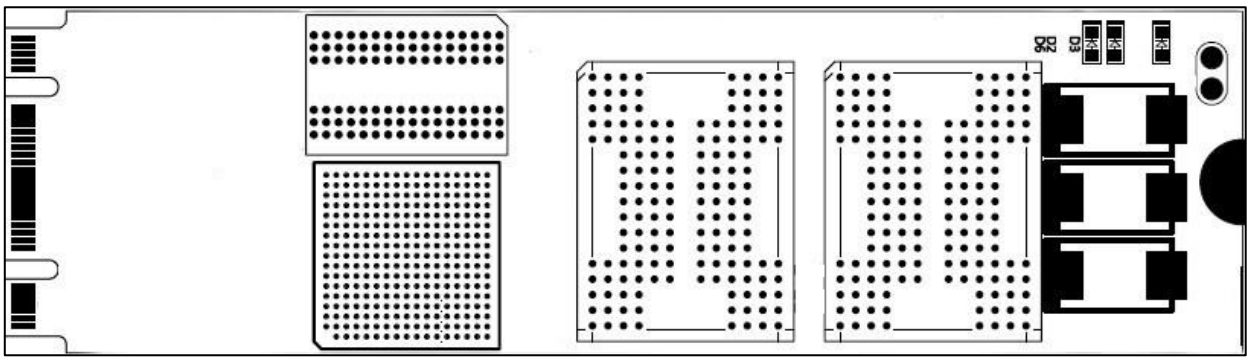


Figure 2 : M.2 2280 SATA3 SSD LED indicator

2.3 Performance

2.3.1 Transfer Modes

- Serial ATA 6.0 Gb/s, backward compatible with Serial ATA 1.5/3.0 Gb/s.

2.3.2 TeraByte Write

Table 3 : TBW Data

Workload	TBW Data							Unit
	64GB	128GB	256GB	512GB	1TB	2TB	3.8TB	
Client	176	352	704	1408	2816	5632	11264	TB
Enterprise	29	58	116	232	465	931	1862	TB

Notice: TBW is estimated by formula **TBW = (Capacity x PE Cycles) x (1 + OP) x (WLE) / (WAF)**

- **OP = (Physical Capacity / Logical Capacity) - 1**
- **WLE =** It could be different depended on the workload or usage containing data size and access rate.
- **Client workload:** Sequential write workload.
- **Enterprise workload:** Follow JESD219A enterprise workload which is generated by VDBENCH script and tested by VDBENCH.

2.3.3 Wear-Leveling

- Enhanced endurance by global Wear-Leveling.

2.4 Environmental Conditions

Table 4 : Environmental Conditions

Feature	Operating	Storage
Temperature (Normal Grade)	-20°C to +75°C	-55°C to +95°C
Temperature (Wide-Temperature Grade)	-40°C to +85°C	-55°C to +95°C
Humidity	10% to 95% RH, non-condensing	
Vibration	20G (Peak-to-Peak), 80~2000 Hz	
Shock	1,500G, 0.5ms	

Notice:

- Vibration: Duration, 30 min x 3 axis.
- Shock: 1500G, 0.5msec, half-sine wave, 3 times in each direction, total = 18 times (6 directions).
- Temperature: The temperature reading is for the environment defined as Ta.

2.5 Reliability

Table 5 : Reliability

Feature	Specification
ECC Capability	Hardware LDPC ECC engine (120bit/1KB)
MTBF	3,000,000 hrs.
Program / Erase Endurance	3,000 P/E cycles
Optimal sustained performance	Direct-To-TLC and SLC Cache Architecture
Data Endurance & Data integrity	StaticDataRefresh technology, Early weak block retirement, Global Wear leveling
Data Retention	10% of program / Erase Endurance cycles: 10 Years
	100% of program / Erase Endurance cycles: 1 Years

Notice:

- Data retention: The value is based on normal program/erase endurance at room temperature. High environmental temperature may shorten the retention period.

2.6 Compliance Specifications

- CE (EN55032 & EN55035)
- FCC Part 15, subpart B
- RoHS 2.0 (2011/65/EU & 2015/863/EU)

2.7 Technique

2.8.1 TCG Opal 2.0

The SLC cache technology divides a cache space in the TLC device to be simulated as an SLC, and the speed in TCG/Opal stands for Trusted Computing Group Opal. The Trusted Computing Group is an organization that develops open standards for trusted computing platforms. The latest Opal Storage Specification is currently available in version 2.0, featuring a demand encryption function for the stored data so that an unauthorized person will not be able to see or access the data, even if possession of a drive was gained.

2.8.2 Thermal Throttling

SP Industrial SSD started implementing a new generation control mechanism of thermal throttling with multiple levels of temperature control. The major benefit of new generation control mechanisms avoids sudden change of SSD performance to get the better balance between performance and thermal management.

2.8.3 Power Shield

The principle of SSD is Power Shield (PS) activates when the external voltage drops to a specific low level, such as from 3.3V to 2.7V. The voltage detection circuit (Voltage Detector) inside the controller will initiate the power supply protection function. When the SSD is operating and the DRAM is powered by an external power supply, the data will be temporarily stored in the DRAM. During the power-off process, the command is sent from the host to the SSD controller to signal that the power is about to be interrupted, and the SSD controller will send confirmation messages to the host, and then transfer the data temporarily stored in the DRAM cache to the Flash Memory. This safeguards the internal firmware and data of the Flash memory from being damaged.

2.8.4 Power Failure Protection

SP Industrial's R series of SSDs implements Advanced PFP with industrial grade polymer capacitors to gain more time for the data flushing process from DRAM cache to FLASH during sudden power-off situations.

2.8.5 Wide Temperature

Products for industrial applications often have to withstand extreme temperature conditions. SP Industrial offers solutions that are able to operate in all systems and environments, including harsh operating environments and industries such as defense and telecommunications. Select SSD controllers from SP Industrial are equipped with wide temperature technology to operate reliably from a wide temperature range of -40°C to +85°C.

2.8.6 Garbage Collection

SSD uses the storage technology of flash memory (NAND flash). The principle of SSD is that the controller stores the data to be written in the Flash memory. When writing data, the SSD must first erase the data in the old block before writing new data. That is, the new data cannot directly cover the old invalid data. For SSD, Garbage Collection refers to the process of re-transferring existing data to other NAND flash locations and erasing useless data.

2.8.7 Wear Leveling

For today's NAND flash devices, the main limitation is Program/Erase lifespan (number of P/E cycles). The key solution for this constraint is to manage the attrition rate in the entire NAND flash device so that each block will be evenly distributed. Therefore, efficient management of wear in whole blocks is required in order to maximize the lifespan of a NAND flash device. To accomplish this, one method is to manage the P/E cycle of each block individually, which will help to regularly distribute them and avoid overlaying on some blocks. This method is called wear leveling.

3. Functional Description

3.1 Architecture

SILICON POWER'S M.2 2280 SATA3 MDC350S/R series is designed to operate and work as data or code storage device by NAND Flash memory and its controller through Standard Serial ATA 6.0Gb/s interface to host systems.

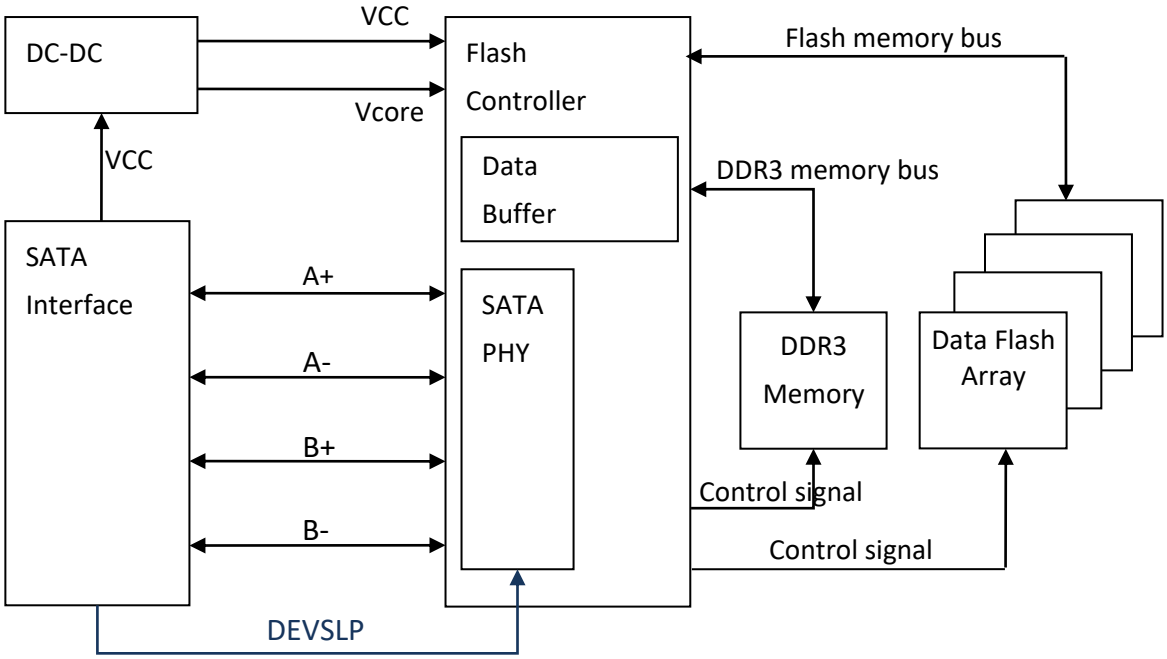


Figure 3 : M.2 2280 SATA3 SSD Block Diagram

3.2 Signal Assignment

The signals assigned for Serial ATA applications are described in the following Figure.

Figure 4 : SATA Signal Connector

Table 6 : M.2 SSD Serial ATA connector pin definitions

Definition	Name	Pin No		Name	Definition
Ground	CONFIG_3	01	02	+3.3V	Supply pin, 3.3 V
Ground	GND	03	04	+3.3V	Supply pin, 3.3 V
No connect	NC	05	06	Not available	No Connect
No connect	NC	07	08	NC	No Connect
No connect	NC	09	10	DAS/DSS	Device Activity Signal / Disable Staggered Spinup
No connect	NC	11	12	Module Key	Mechanical notch B
Mechanical notch B	Module Key	13	14	Module Key	Mechanical notch B
Mechanical notch B	Module Key	15	16	Module Key	Mechanical notch B
Mechanical notch B	Module Key	17	18	Module Key	Mechanical notch B
Mechanical notch B	Module Key	19	20	Not Available	No Connect
Ground	CONFIG_0	21	22	Not available	No Connect
No Connect	Not availabl e	23	24	Not available	No Connect
No Connect	Not availabl e	25	26	Not available	No Connect
Ground	GND	27	28	Not available	No Connect
No Connect	Not availabl e	29	30	Not available	No Connect
No Connect	Not availabl e	31	32	Not available	No Connect
Ground	GND	33	34	Not available	No Connect
No Connect	Not availabl e	35	36	Not available	No Connect
No Connect	Not availabl e	37	38	DEVSLP	Device Sleep
Ground	GND	39	40	Not available	No Connect
Host receiver differential signal pair of SSD	SATA B+	41	42	Na	No Connect
Host receiver differential signal pair of SSD	SATA B-	43	44	Not available	No Connect
Ground	GND	45	46	Not available	No Connect
Host transmitter differential sig nal pair of SSD	SATA A-	47	48	NC	No Connect
Host transmitter differential sig nal pair of SSD	SATA A+	49	50	PERST#	No Connect
Ground	GND	51	52	NC	No Connect

No Connect	NC	53	54	NC	No Connect
No Connect	NC	55	56	Reserved	No Connect
Ground	GND	57	58	Reserved	No Connect
Mechanical notch M	Module Key	59	60	Module Key	Mechanical notch M
Mechanical notch M	Module Key	61	62	Module Key	Mechanical notch M
Mechanical notch M	Module Key	63	64	Module Key	Mechanical notch M
Mechanical notch M	Module Key	65	66	Module Key	Mechanical notch M
No Connect	NC	67	68	SUSCLK	No Connect
Ground	CONFIG_1	69	70	+3.3V	Supply pin, 3.3 V
Ground	GND	71	72	+3.3V	Supply pin, 3.3 V
Ground	GND	73	74	+3.3V	Supply pin, 3.3 V
Ground	CONFIG_2	75			

NOTICE: DEVSLP function is depended on Host supporting.

3.3 Dual Secure Design for Power Failure Protection

Silicon Power implemented dual secure design for power failure protection

- Power shielding firmware architecture protection when sensing unstable voltage and power down to stop receiving host commands. (All series)
- Implement Advanced PFP with industrial grade polymer capacitors to gain more time for the data flushing process from DRAM cache to Flash, under sudden power off situations. (R series only)

How SSD controller manage power failure?

- (A) SSD FW stored inside NAND Flash called system block. When System power on, SSD will load related mapping table and initial commands into DRAM for SSD controller.
- (B) When VCC is under 4V, SSD Controller will enable the power shielding function, during this period the SSD controller will start to flush DRAM cache data save into FLASH to secures the user data in a limit time.
- (C) At the same time VCC <4V SSD controller will stop receiving command from Host to protect itself. Host can not recognize SSD and SSD stop working during this period until VCC resumes and become stable.
- (D) When VCCF is under 2.7V, SSD controller will initial flush command to write back mapping table back to flash system block. During this period Host can not recognize SSD. SSD still can not work even power resumes. Need to turn Power ON/OFF again for host to restart SSD work normally
- During SSD operation, data is temporarily stored in the DRAM cache to reduce the performance gap between the host interface and the NAND Flash memory. However, in cases of unexpected sudden power loss, such as unplugging the power to the system, sudden battery loss or unplugging devices from the system, the flushing process cannot be completed and may cause serious device failure. Silicon Power Dual secure design for power failure protection (PFP) resolves such issue with firmware-based protect mechanism and capacitor backup circuit.

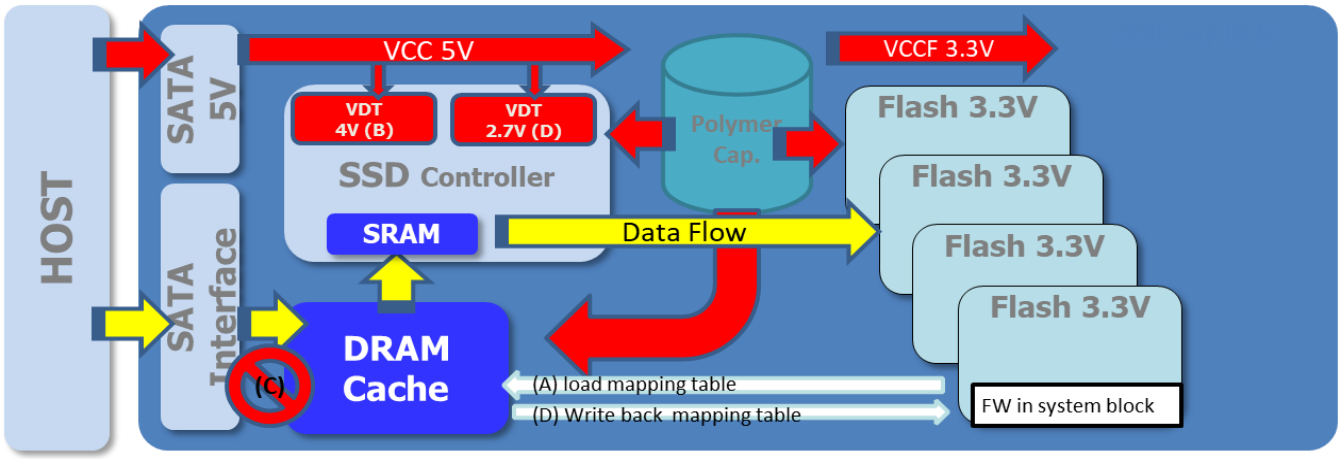


Figure 5 : How does SSD controller manage power failure?

How Power Failure Protection mechanism works?

- Power Shielding function integrates built-in VDT and firmware mechanism. The trigger alert can monitor abnormal power drop and take instant actions, such as prohibit receiving data from host and backup mapping/ link table into Flash, once a possible power failure is detected.
- Advanced PFP is a way to gain more time for the data flushing process from DRAM cache to Flash, under sudden power off situations by using dedicated polymer capacitor components. These capacitors are charged during power on and offer charged power to the SSD circuit when external power is off.
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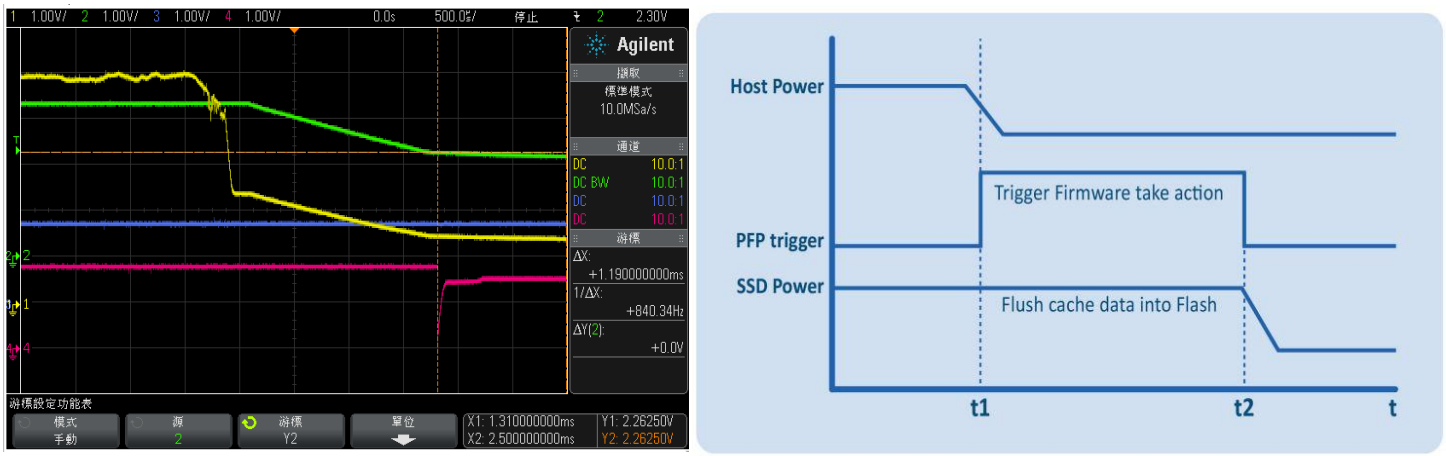

Figure 6 : How Power Failure Protection mechanism works?

3.4 Support ATA Commands

The table showed below summarizes the supported ATA command set. For detail description of the commands, please check the ATA standard or contact Silicon Power local representatives for the helps.

Table 7 : ATA Command List

No	Command Set	Code	FR	SC	SN	CY	DH	LBA
General Feature Set								
1	Execute Drive Diagnostic Mode	90h	-	-	-	-	D	-
2	Flush Cache	E7h	-	-	-	-	D	-
3	Identify Device	ECh	-	-	-	-	D	-
4	Initialize Device Parameters	91h	-	Y	-	-	Y	-
5	NOP	00h	-	-	-	-	D	-
6	Read Buffer	E4h	-	-	-	-	D	-
7	Read DMA	C8h	-	Y	Y	Y	Y	Y
8	Read Multiple	C4h	-	Y	Y	Y	Y	Y
9	Read Sector(s)	20h	-	Y	Y	Y	Y	Y
10	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
11	Seek	7xh	-	Y	-	Y	Y	Y
12	Set Feature	EFh	Y	-	-	-	D	-
13	Set Multiple Mode	C6h	-	Y	-	-	D	-
14	Write Buffer	E8h	-	-	-	-	D	-
15	Write DMA	CAh	-	Y	Y	Y	Y	Y
16	Write Multiple	C5h	-	Y	Y	Y	Y	Y
17	Write Sector(s)	30h	-	Y	Y	Y	Y	Y
48-bit Address Feature Set								
18	Flush Cache Ext	EAh	-	-	-	-	D	-
19	Read DMA Ext	25h	-	Y	Y	Y	Y	Y
20	Read Multiple Ext	29h	-	Y	Y	Y	Y	Y
21	Read Sector(s) Ext	24h	-	Y	Y	Y	Y	Y
22	Read Verify Sector(s) Ext	42h	-	Y	Y	Y	Y	Y
23	Write DMA Ext	35h	-	Y	Y	Y	Y	Y
24	Write DMA FUA Ext	3Dh	-	Y	Y	Y	Y	Y
25	Write Multiple Ext	39h	-	Y	Y	Y	Y	Y
26	Write Multiple FUA Ext	CEh	-	Y	Y	Y	Y	Y
27	Write Sector(s) Ext	34h	-	Y	Y	Y	Y	Y
Host Protected Area (HPA) Feature Set (Option)								
28	Read Native Max Address	F8h	-	-	-	-	D	-
29	Read Native Max Address Ext	27h	-	-	-	-	D	-
30	Set Max Address	F9h	-	Y	Y	Y	Y	Y
31	Set Max Address Ext	37h	-	Y	Y	Y	Y	Y
32	Set Max Freeze Lock	F9h	04h	-	-	-	D	-
33	Set Max Lock	F9h	02h	-	-	-	D	-
34	Set Max Set Password	F9h	01h	-	-	-	D	-
35	Set Max Unlock	F9h	03h	-	-	-	D	-
Power Management Feature Set								
36	Check Power Mode	E5h or 98h	-	-	-	-	D	-
37	Idle	E3h or 97h	-	Y	-	-	D	-
38	Idle Immediate	E1h or 95h	-	-	-	-	D	-
39	Sleep	E6h or 99h	-	-	-	-	D	-

40	Standby	E2h or 96h	-	-	-	-	D	-
41	Standby Immediate	E0h or 94h	-	-	-	-	D	-
Security Mode Feature Set								
42	Security Disable Password	F6h	-	-	-	C	-	-
43	Security Erase Prepare	F3h	-	-	-	C	-	-
44	Security Erase Unit	F4h	-	-	-	C	-	-
45	Security Freeze Lock	F5h	-	-	-	C	-	-
46	Security Set Password	F1h	-	-	-	C	-	-
47	Security Unlock	F2h	-	-	-	C	-	-
SMART Feature Set								
48	SMART Disable Operations	B0h	D9h	Y	-	Y	Y	-
49	SMART Enable/Disable Autosave	B0h	D2h	Y	-	Y	Y	-
50	SMART Enable Operations	B0h	D8h	Y	-	Y	Y	-
51	SMART Execute Off-Line Immediate	B0h	D4h	Y	-	Y	Y	-
52	SMART Read Data	B0h	D0h	Y	-	Y	Y	-
53	SMART Read Threshold	B0h	D1h	Y	-	Y	Y	-
54	SMART Return Status	B0h	DAh	Y	-	Y	Y	-
55	SMART Save Attribute Values	B0h	D3h	Y	-	Y	Y	-

Definitions:

FR = Features register **SN** = Sector number register **DH** = Device/drive/head register

CY = Cylinder registers **SC** = Sector count register **D** = Only the device parameter is valid and not the head parameter

LBA = Logical block address mode supported (see command descriptions for use).

Y - The register contains a valid parameter for this command. For the drive/head register Y means both the device and head parameters are used.

C - The register contains command specific data (see command descriptions for use).

3.5 Device Identification

The following is the device identify table.

Table 8 : Identify Device Information

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information	
0	0044h	2		General configuration – Bit Significant with ATA definitions.	
			F	15	0:ATAdevice
			X	14-8	Retired
			F	7	1:removablemediadevice
			X	6	Obsolete
			X	5-3	Retired
			F	2	Response incomplete
			X	1	Retired
			F	0	Reserved
1	XXXXh	2	X	Default number of cylinders	
2	0000h	2	V	Reserved	
3	00XXh	2	X	Default number of heads	
4-5	XXXXh	4	X	Reserved	
6	XXXXh	2	X	Default number of sectors per track	
7-8	XXXXh	4	V	Reserved for assignment by the CFA	
9	0000h	2	X	Reserved	
10-19	Aaaa	20	F	Serial number in ASCII (Right Justified)	
20-21	XXXXh	4	X	Reserved	
22	XXXXh	2	X	Reserved	
23-26	aaaa	8	F	Firmware revision in ASCII. Big Endian Byte Order in Word	
27-46	aaaa	40	F	Model number in ASCII (Left Justified) Big Endian Byte Order in Word	
47	8001h	2		Maximum number of sectors on Read/Write Multiple command	
			F	15-8	80h: Fixed
			F	7-0	00h: Reserved
					01h: Maximum number of 1 sectors on READ/WRITE MULTIPLE commands
48	XXXXh	2	X	Reserved	
49	0F00h	2		Capabilities: DMA, LBA, IORDY supported	
			F	15-14	Reserved for the IDENTIFY PACKET DEVICE command.
			F	13	1: Standby timer values as specified in this standard are supported
					0: Standby timer values shall be managed by the device
			F	12	Reserved for the IDENTIFY PACKET DEVICE command
			F	11	1: IORDY supported
					0: IORDY may be supported
			F	10	1: IORDY may be disabled
			F	9	1: LBA supported
			F	8	1: DMA supported
			X	7-0	Retired
50	4000h	2		Capabilities: Others, Fixed	
			F	15	Shall be cleared to zero.
			F	14	Shall be set to one.
			F	13-2	Reserved.
			X	1	Obsolete
			F	0	Shall be set to one to indicate a device specific Standby timer value minimum
51	0200h	2		PIO data transfer cycle timing mode 2	

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information	
			X	15-8	PIO data transfer cycle timing mode
			X	7-0	Reserved
52	XXXXh	2	X	Reserved	
53	0007h	2		Data Fields 54 to 58, 64 to 70 and 88 are valid	
			F	15-3	Reserved
			F	2	1: the fields reported in word 88 are valid
					0: the fields reported in word 88 are not valid
			F	1	1: the fields reported in words 70:64 are valid
					0: the fields reported in words 70:64 are not valid
			X	0	1: the fields reported in words 58:54 are valid
					0: the fields reported in words 58:54 are not valid
54	XXXXh	2	X	Current numbers of cylinders	
55	00XXh	2	X	Current numbers of heads	
56	XXXXh	2	X	Current sectors per track	
57-58	XXXXh	4	X	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)	
59	0100h	2		Multiple sector setting	
			F	15-9	Reserved
			V	8	1: Multiple sector setting is valid
			V	7-0	xxh: Setting for number of sectors that shall be transferred per interrupt on R/W Multiple command
60-61	XXXXh	4	F	Total number of sectors addressable in LBA Mode	
62	0000h	2	X	Reserved	
63	0007h	2		Multiword DMA transfer.	
			F	15-11	Reserved
			V	10	1: Multiword DMA mode 2 is selected
					0: Multiword DMA mode 2 is not selected
			V	9	1: Multiword DMA mode 1 is selected
					0: Multiword DMA mode 1 is not selected
			V	8	1: Multiword DMA mode 0 is selected
					0: Multiword DMA mode 0 is not selected
			F	7-3	Reserved
			F	2	1: Multiword DMA mode 2 and below are supported
			F	1	1: Multiword DMA mode 1 and below are supported
			F	0	1: Multiword DMA mode 0 is supported
64	0003h	2		Advanced PIO modes 3 and 4 supported	
			F	15-8	Reserved
			F	7-0	Advanced PIO modes supported
65	0078h	2	F	Minimum Multiword DMA transfer cycle time per word.	
				15-0	Cycle time in ns.
66	0078h	2	F	Recommended Multiword DMA transfer cycle time.	
				15-0	Cycle time in ns.
67	0078h	2	F	Minimum PIO transfer cycle time without flow control.	
				15-0	Cycle time in ns.
68	0078h	2	F	Minimum PIO transfer cycle time with IORDY flow control	
				15-0	Cycle time in ns.
69-70	0000h	4	F	Reserved	
71-74	0000h	8	F	Reserved for Identify Packet Device Command	
75	0000h	2		Queue depth	
			F	15-5	Reserved
			F	4-0	Maximum queue depth - 1
76	0206h	2		Serial ATA Capabilities	

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information	
			F	15-11	Reserved for Serial ATA
			F	10	1: supports PHY Event Counts
			F	9	1: supports receipt of Host initiated power management requests
			F	8	1: supports NCQ Feature Set
			F	7-3	Reserved for Serial ATA
			F	2	1: supports SATA Gen2 Signaling Speed (3.0Gb/s)
			F	1	1: supports SATA Gen1 Signaling Speed (1.5Gb/s)
			F	0	Shall be cleared to zero
77	0000h	2	X	Reserved for Serial ATA	
78	0008h	2		Serial ATA Feature Supported	
			F	15-7	Reserved for Serial ATA
			F	6	1: supports Software Settings Preservation
			F	5	Reserved for Serial ATA
			F	4	1: supports in-order data delivery
			F	3	1: supports initiating power management
			F	2	1: Supports DMA setup auto-activation
			F	1	1: Supports none-zero buffer offset
			F	0	Shall be cleared to zero
79	0000h	2		Serial ATA Feature Enabled	
			F	15-7	Reserved for Serial ATA
			F	6	1: Software Settings Preservation enabled
			F	5	Reserved for Serial ATA
			F	4	1: In-order data delivery enabled
			F	3	1: Initiating power management enabled
			F	2	1: DMA setup auto-activation enabled
			F	1	1: None-zero buffer offset enabled
			F	0	Shall be cleared to zero
80	01FCh	2		Major version number, ATA-8 support	
			F	15	Reserved
			F	14	Reserved for ATA/ATAPI-14
			F	13	Reserved for ATA/ATAPI-13
			F	12	Reserved for ATA/ATAPI-12
			F	11	Reserved for ATA/ATAPI-11
			F	10	Reserved for ATA/ATAPI10
			F	9	Reserved for ATA/ATAPI-9
			F	8	1: supports ATA/ATAPI-8
			F	7	1: supports ATA/ATAPI-7
			F	6	1: supports ATA/ATAPI-6
			F	5	1: supports ATA/ATAPI-5
			F	4	1: supports ATA/ATAPI-4
			F	3	Obsolete
			F	2	Obsolete
			F	1	Obsolete
			F	0	Reserved
81	0000h	2	F	Minor version number	
82	742Bh	2		Features/command sets supported (NOP, SMART,…)	
			X	15	Obsolete
			F	14	1: NOP command supported
			F	13	1: READ BUFFER command supported
			F	12	1: WRITE BUFFER command supported
			X	11	Obsolete

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information	
			F	10	1: Host Protected Area feature set supported
			F	9	1: DEVICE RESET command supported
			F	8	1: SERVICE interrupt supported
			F	7	1: release interrupt supported
			F	6	1: look-ahead supported
			F	5	1: write cache supported
			F	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
			F	3	1: mandatory Power Management feature set supported
			F	2	1: Removable Media feature set supported
			F	1	1: Security Mode feature set supported
			F	0	1: SMART feature set supported
83	7500h	2		Features/command sets supported (Flush Cache, …)	
			F	15	Shall be cleared to zero
			F	14	Shall be set to one
			F	13	Reserved
			F	12	Shall be set to one to indicate that the mandatory FLUSH CACHE command is supported
			F	11	1: DCO feature set is supported
			F	10	1: 48-bit Address feature set is supported
			F	9	1: AAM feature set is supported
			F	8	1: SET MAX security extension supported
			F	7	Reserved
			F	6	1: SET FEATURES subcommand required to spin up after power-up
			F	5	1: Power-Up In Standby feature set supported
			F	4	1: Removable Media Status Notification feature set supported
			F	3	1: Advanced Power Management feature set supported
			F	2	1: CFA feature set supported
			F	1	1: READ/WRITE DMA QUEUED supported
			F	0	1: DOWNLOAD MICROCODE command supported
84	4002h	2		Features/command sets supported (extension)	
			F	15	Shall be cleared to zero
			F	14	Shall be set to one
			F	13	1: IDLE IMMEDIATE command with UNLOAD feature is supported
			F	12-11	Reserved for 3D NAND
			F	10-9	Obsolete
			F	8	1: 64-bit World wide name is supported
			F	7	1: WRITE DMA QUEUED FUA EXT command is supported
			F	6	1: WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported
			F	5	1: GPL feature set is supported
			F	4	1: Streaming feature set is supported
			F	3	1: Media Card Pass Through Command feature set is supported
			F	2	1: Media serial number is supported
			F	1	1: SMART self-test supported
			F	0	1: SMART error logging supported
85	XXXXh	2		Features/command sets enabled (NOP, SMART,…)	
			X	15	Obsolete
			F	14	1: NOP command enabled
			F	13	1: READ BUFFER command enabled

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information	
			F	12	1: WRITE BUFFER command enabled
			X	11	Obsolete
			V	10	1: Host Protected Area feature set enabled
			F	9	Shall be cleared to zero to indicate that the DEVICE RESET command is not supported
			V	8	1: SERVICE interrupt enabled
			V	7	1: release interrupt enabled
			V	6	1: look-ahead enabled
			V	5	1: write cache enabled
			F	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
			F	3	Shall be set to one to indicate that the mandatory Power Management feature is supported
			X	2	Obsolete
			V	1	1: Security feature set enabled
			V	0	1: SMART feature set enabled
86	XXXXh	2		Features/command sets enabled (Flush Cache, …)	
			F	15	1: Word 119-120 are valid
			F	14	Reserved
			F	13	1: FLUSH CACHE EXT command supported
			F	12	1: FLUSH CACHE command supported
			F	11	1: DCO feature set is supported
			F	10	1: 48-bit Address feature set is supported
			V	9	1: AAM feature set is supported
			V	8	1: SET MAX security extension enabled by SET MAX SET PASSWORD
			X	7	Reserved for Address Offset Reserved Area Boot Method
			F	6	1: SET FEATURES subcommand required to spin-up after power-up
			V	5	1: Power-Up In Standby feature set enabled
			X	4	Obsolete
			V	3	1: Advanced Power Management feature set enabled
			F	2	1: CFA feature set is supported
			F	1	1: TCQ feature set is supported
			F	0	1: DOWNLOAD MICROCODE command supported
87	XXXXh	2		Features/command sets enabled (extension)	
			F	15	Shall be cleared to zero
			F	14	Shall be set to one
			F	13	1: The IDLE IMMEDIATE command with UNLOAD feature is supported
			X	12-11	Reserved for 3D NAND
			X	10-9	Obsolete
			F	8	1: 64-bit World wide name is supported
			F	7	1: WRITE DMA QUEUED FUA EXT command is supported
			F	6	1: WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported
			F	5	1: GPL feature set is supported
			X	4	Obsolete
			V	3	1: Media Card Pass Through Command feature set is supported
			V	2	1: Media serial number is supported
			F	1	1: SMART self-test supported
			F	0	1: SMART error logging supported
88	007Fh	2		Ultra DMA Mode Supported and Selected	

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information	
			F	15	Reserved
			V	14	1: Ultra DMA mode 6 is selected
					0: Ultra DMA mode 6 is not selected
			V	13	1: Ultra DMA mode 5 is selected
					0: Ultra DMA mode 5 is not selected
			V	12	1: Ultra DMA mode 4 is selected
					0: Ultra DMA mode 4 is not selected
			V	11	1: Ultra DMA mode 3 is selected
					0: Ultra DMA mode 3 is not selected
			V	10	1: Ultra DMA mode 2 is selected
					0: Ultra DMA mode 2 is not selected
			V	9	1: Ultra DMA mode 1 is selected
					0: Ultra DMA mode 1 is not selected
			V	8	1: Ultra DMA mode 0 is selected
					0: Ultra DMA mode 0 is not selected
			F	7	Reserved
			F	6	1: Ultra DMA mode 6 and below are supported
			F	5	1: Ultra DMA mode 5 and below are supported
			F	4	1: Ultra DMA mode 4 and below are supported
			F	3	1: Ultra DMA mode 3 and below are supported
			F	2	1: Ultra DMA mode 2 and below are supported
			F	1	1: Ultra DMA mode 1 and below are supported
			F	0	1: Ultra DMA mode 0 is supported
89	0003h	2	X	15-8	Reserved
			F	7-0	Time required for security erase unit completion
90	0000h	2	X	15-8	Reserved
			F	7-0	Time required for Enhanced security erase completion
91	0000h	2	V	Current advanced power management value	
92	FFFEh	2	V	Master Password Identifier	
93-99	0000h	14	X	Reserved	
100-103	VVVVh	8	V	Total Number of User Addressable Logical Sectors for 48-bit commands (QWord)	
104-127	0000h	48	V	Reserved	
128	0001h	2		Security status	
			F	15-9	Reserved
			V	8	Security level 0: High, 1: Maximum
			X	7-6	Reserved
			F	5	1: Enhanced security erase supported
			V	4	1: Security count expired
			V	3	1: Security frozen
			V	2	1: Security locked
			V	1	1: Security enabled
			F	0	1: Security supported
129-159	0000h	62	X	Reserved for vendor	
160	0000h	2		CFA power mode	
			F	15	Word 160 supported
			X	14	Reserved
			F	13	CFA power mode 1 is required for one or more commands implemented by the device
			V	12	CFA power mode 1 disabled
			F	11-0	Maximum current in mA

Word Address	Default Value	Total Bytes	F/V	Data Field Type Information	
161-175	0000h	30	X	Reserved for Compact Flash Association	
176-216	0000h	82	V	Reserved	
217	0001h	2	F	Nominal media rotation rate	
218-254	0000h	74	X	Reserved	
255	VVVVh	2		Integrity Word	
			V	15-8	Checksum
			V	7-0	Signature

NOTICE:

1. F/V: Fixed/Variable content.
2. F: The content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.
V: The contents of the word are variable and may change depending on the state of the device or the commands executed by the device.
X: The content of the word may be fixed or variable.

3.6 Set Feature Command

The table listed below is the supported feature field set in feature register

Table 9 : SET FEATURES Feature Field Definitions

Value	Function
02h	Enable volatile write cache
03h	Set transfer mode
05h	Enable the APM feature set
10h	Enable use of SATA feature
55h	Disable read look-ahead feature
66h	Disable reverting t power on defaults by soft reset
82h	Disable volatile write cache
85h	Disable the APM feature set
90h	Disable use of SATA feature
AAh	Enable read look-ahead feature
CCh	Enable reverting to power-on defaults

The effective SATA features are defined as below:

Table 10 : SATA Features

Sector Count Value	Description
02h	DMA Setup FIS Auto-Active optimization
03h	Device-Initiated interface power state transitions
06h	Software Settings Preservation

3.7 SMART Feature Command

SILICON POWER'S M.2 2280 SATA MDC350 series supports SMART function. It response the up-to-date SMART command set with the SMART data structure as following:

Table 11 : SMART Feature Registers Values

Value	Command
D0h	SMART Read Data
D1h	Read Attribute Threshold
D2h	SMART Enable/Disable Attribute Autosave
D3h	Save Attribute Values
D4h	Execute Off-Line Immediate
D8h	SMART Enable Operations
D9h	SMART Disable Operations
DAh	SMART Return Status
Others	Reserved

Table 12: Device SMART Data Structure

Offset	Description
0-1	SMAT Structure Revision code
2-361	Attribute entries 1 to 30 (12 bytes each)
362	Off-line data collection status (No off-line data collection) (Fixed)
363	Self-test execution status byte (Self-test completed) (Fixed)
364-365	Total time in seconds to complete off-line data collection activity (Fixed)
366	Reserved
367	Off-line data collection capability (No Off-line data collection) (Fixed)
368-369	SMART capability
370	Error logging capability (No error logging) (Fixed)
371	Reserved
372	Short self-test routine recommended polling time (in minutes) (Fixed)
373	Extended self-test routine recommended polling time (in minutes) (Fixed)
374-510	Reserved
511	Data structure checksum

- (0-1) Revision code

  This revision code area defines the firmware revision for the device.

- (2-361) Attribute entries 1 to 30 (12 bytes each)

  There are five attributes that are defined for this device. These return their data in the attribute section of the SMART data, using a 12 byte data field. Rest of the area is reserved. The Individual attribute data structure is defined as following:

Offset	+0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
Attribute	ID	Flag		Init	Worst	Raw Attribute Value						Rsv
Read Error Rate	01h	00h	00h	64h	64h	(1)	00h	00h	00h	00h	00h	00h
Reallocated Sectors Count	05h	00h	00h	64h	64h	(2)		00h	00h	00h	00h	00h
Power Cycle Count	0Ch	00h	00h	64h	64h	(3)		00h	00h	00h	00h	00h
Uncorrectable SC when R/W	A0h	00h	00h	64h	64h	(4)				00h	00h	00h
No. of Valid Spare Block	A1h	00h	00h	64h	64h	(5)		00h	00h	00h	00h	00h
No. of Valid Child Pair	A2h	00h	00h	64h	64h	(6)		00h	00h	00h	00h	00h
No. of Initial Invalid Block	A3h	00h	00h	64h	64h	(7)		00h	00h	00h	00h	00h
Total Erase Count	A4h	00h	00h	64h	64h	(8)				00h	00h	00h
Max. Erase Count	A5h	00h	00h	64h	64h	(9)				00h	00h	00h
Min. Erase Count	A6h	00h	00h	64h	64h	(10)				00h	00h	00h
Average Erase Count	A7h	00h	00h	64h	64h	(11)				00h	00h	00h
Power-off retract Count	C0h	00h	00h	64h	64h	(12)				00h	00h	00h
H/W ECC Recovered	C3h	00h	00h	64h	64h	(13)				00h	00h	00h
Reallocation Event Count	C4h	00h	00h	64h	64h	(14)				00h	00h	00h
UDMA CRC Error Count	C7h	00h	00h	64h	64h	(15)		00h	00h	00h	00h	00h
Total LBAs Written (unit: 32MB)	F1h	00h	00h	64h	64h	(16)				00h	00h	00h
Total LBAs Read (unit: 32MB)	F2h	00h	00h	64h	64h	(17)				00h	00h	00h

Notice:

1. Use "Little Indian" rule. If the data is in two bytes length, LSB is in lower bytes and MSB is in higher byte. All of the data are in HEX format.

2. The entries with other indices are reserved for controller vendor specific usage.

- (368-369) SMART capabilities

  The following describes the definition for the SMART capabilities bits.

  - Bit 0 - If this bit is set to one, the device saves SMART data prior to going into a power saving mode (Idle, Standby, or Sleep) or immediately upon return to Active or Idle mode from a Standby mode. If this bit is cleared to zero, the device does not save SMART data prior to going into a power saving mode (Idle, Standby, or Sleep) or immediately upon return to Active or Idle mode from a Standby mode.
  - Bit 1 - This bit shall be set to one to indicate that the device supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.
  - Bits (15:2) (Reserved).

- (372-373) Self-test routine recommended polling time

  The self-test routine recommended polling time shall be equal to the number of minutes that is the minimum recommended time before which the host should first poll for test completion status. Actual test time could be several times this value. Polling before this time could extend the self-test execution time or abort the test depending on the state of bit 2 of the off-line data capability bits.

- (511) Data structure checksum

  The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes will be zero when the checksum is correct. The checksum is placed in byte 511.

4. Ordering Information

4.1 Part Number Definition

Table 13 : Part Number Definition

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	S	P	0	3	8	T	I	M	D	C	3	5	5	S	V	0

Code 1-2: Brand	SP: Silicon Power
Code 3-6: Capacity	064G: 64GB; 128G: 128GB; 256G: 256GB; 512G: 512GB; 010T: 1TB; 020T: 2TB; 038T: 3.8TB
Code 7: Product	I: Industrial Grade Product
Code 8-10: Type & Form Factor	MDC: SATA M.2 2280
Code 11-13: Model Series	355: WD (3D TLC)
Code 14: SSD Series	S: SSD with DRAM
Code 15: Operation Temperature	V: Normal temperature -20°C to +75°C W: Wide temperature -40°C to +85°C
Code 16: Reserved	0: Standard

4.2 Standard M.2 2280 SATA3 MDC350S Series Information

Capacity	Part Number	BOM Code	Description	R/W Performance	
				Maximum (MB/s)	IOPS
Normal Temperature (-20°C ~75°C)					
64GB	SP064GIMDC355SV0	064GIMDC355SV0-060	BiCS4 512Gb*1	390/200	25K/18K
128GB	SP128GIMDC355SV0	128GIMDC355SV0-070	BiCS5 512Gb*2	320/230	22K/18K
128GB	SP128GIMDC355SV0	128GIMDC355SV0-080	BiCS5 512Gb*2	325/270	84K/80K
256GB	SP256GIMDC355SV0	256GIMDC355SV0-060	BiCS5 1Tb*2	560/480	39K/43K
256GB	SP256GIMDC355SV0	256GIMDC355SV0-070	BiCS5 1Tb*2	560/485	83K/80K
512GB	SP512GIMDC355SV0	512GIMDC355SV0-050	BiCS5 1Tb*4	560/500	89K/79K
512GB	SP512GIMDC355SV0	512GIMDC355SV0-060	BiCS5 1Tb*4	560/515	90K/81K
1TB	SP010TIMDC355SV0	010TIMDC355SV0-030	BiCS5 2Tb*4	540/310	80K/77K
1TB	SP010TIMDC355SV0	010TIMDC355SV0-040	BiCS5 2Tb*4	560/515	92K/81K
2TB	SP020TIMDC355SV0	020TIMDC355SV0-010	BiCS5 4Tb*4	540/310	80K/77K
2TB	SP020TIMDC355SV0	020TIMDC355SV0-020	BiCS5 4Tb*4	560/510	85K/81K

3.8TB	SP038TIMDC355SV0	038TIMDC355SV0-010	BiCS5 8Tb*4	540/480	91K/80K
Wide Temperature (-40°C ~ 85°C)					
128GB	SP128GIMDC355SW0	128GIMDC355SW0-010	BiCS5 512Gb*2	320/230	22K/18K
256GB	SP256GIMDC355SW0	256GIMDC355SW0-010	BiCS5 1Tb*2	560/480	39K/43K
512GB	SP512GIMDC355SW0	512GIMDC355SW0-010	BiCS5 1Tb*4	560/500	89K/79K
1TB	SP010TIMDC355SW0	010TIMDC355SW0-010	BiCS5 2Tb*4	540/310	80K/77K
2TB	SP020TIMDC355SW0	020TIMDC355SW0-010	BiCS5 4Tb*4	540/310	80K/77K

4.3 Ordering Information of M.2 2280 SATA3 MDC350R series

Capacity	Part Number	BOM Code	Description	R/W Performance	
				Maximum (MB/s)	IOPS
Normal Temperature (-20°C ~75°C)					
128GB	SP128GIMDC355RV0	128GIMDC355RV0-020	BiCS4 1Tb*2	390/200	25K/18K
256GB	SP256GIMDC355RV0	256GIMDC355RV0-020	BiCS4 1Tb*2	560/520	74K/54K
512GB	SP512GIMDC355RV0	512GIMDC355RV0-010	BiCS4 1Tb*4	560/520	79K/70K
1TB	SP010TIMDC355RV0	010TIMDC355RV0-010	BiCS4 2Tb*4	560/520	94K/89K
Wide Temperature (-40°C ~85°C)					
128GB	SP128GIMDC355RW0	128GIMDC355RW0-010	BiCS5 512Gb*2	320/230	22K/18K
256GB	SP256GIMDC355RW0	256GIMDC355RW0-010	BiCS5 1Tb*2	560/480	39K/43K
512GB	SP512GIMDC355RW0	512GIMDC355RW0-010	BiCS5 1Tb*4	560/500	89K/79K
1TB	SP010TIMDC355RW0	010TIMDC355RW0-010	BiCS5 2Tb*4	540/310	80K/77K
2TB	SP020TIMDC355RW0	020TIMDC355RW0-010	BiCS5 4Tb*4	540/310	80K/77K

4.4 Appendix

Table 14 : Abbreviation

Item	Abbreviation	Description
1	PCIe	Peripheral Component Interconnect Express
2	NVMe	Non-Volatile Memory Express
3	Gen	Generation
4	TBW	Tera Byte Write
5	MTBF	Mean Time Between Failures
6	LDPC	Low Density Parity Check
7	RAID	Redundant Array of Independent Drives
8	ECC	Error Correction Code
9	TCG	Trusted Computing Group
10	SMART	Self-Monitoring Analysis and Reporting Technology
11	FDE	Full Disk Encryption
12	AES	Advanced Encryption Standard
13	SLC	Single-Level Cell
14	SSD	Solid State Disk
15	OP	Over Provisioning
16	PS	Power Shield
17	DC	Direct Current
18	LED	Light Emitting Diode
19	DRAM	Dynamic Random Access Memory
20	PE	Program/Erase
21	WAF	Write Amplification Factor
22	WLE	Wear Leveling Efficiency
23	Ta	Ambient Temperature
24	LBA	Logical Block Address

Contact Information

Silicon Power Computer & Communications Incorporation, a solid state memory or storage business company, provides total solutions in the design and marketing of SSD, Flash Module, and Industry Card products. For further supporting or detail information related to the products, please inform us through the following contact email address: isupport@silicon-power.com. We will response the requests soon.